AMENDMENTS TO THE CLAIMS

Please amend the claims as follows:

Following is a list of the currently pending claims:

1. (Previously Presented) A processor, comprising:

a plurality of pipelined functional units for executing instructions;

a scheduler, coupled to the plurality of functional units, wherein the scheduler is programmed to, in a first stage, map each of at least two separate instruction groups to at least a portion of the functional units independently of each other, and based at least in part on functional unit availability and instruction dependencies, perform a merging and remapping of the at least two separate instruction groups to the at least a portion of the functional units in a second stage.

2. (Original) The processor of claim 1, wherein the scheduler is programmed to deliver the instructions to the portion of functional units following merging and remapping.

3. (Canceled)

4. (Previously Presented) The processor of claim 1, wherein the at least a portion of the functional units execute instructions from the at least two instruction groups.

5. (Original) The processor of claim 1, wherein the instruction groups follow a

simultaneous multi-threading structure.

6. (Original) The processor of claim 1, wherein the instruction groups are prioritized to prevent pipeline failures during execution of instructions.

7. (Previously Presented) A machine-readable medium having stored thereon a plurality of executable instructions, the plurality of instructions comprising instructions to:

in a first stage, map each of at least two separate instruction groups to at least a portion of functional units independently of each other; and

based at least in part on functional unit availability and instruction dependencies, perform a merging and remapping of the at least two separate instruction groups to the at least a portion of functional units in a second stage.

8. (Original) The medium of claim 7, wherein said instructions include instructions to deliver the instructions to the portion of functional units following merging and remapping.

9. (Canceled)

10. (Previously Presented) The medium of claim 7, wherein the at least a portion of functional units execute instructions from the at least two instruction groups.

11. (Original) The medium of claim 7, wherein the instruction groups follow a simultaneous multi-threading structure.

12. (Original) The medium of claim 7, wherein the instruction groups are prioritized to prevent pipeline failures during execution of instructions.

13. (Previously Presented) A method for dispersing instructions to executed by a processor, comprising:

in a first stage, mapping each of at least two separate instruction groups to at least a portion of functional units independently of each other; and

based at least in part on functional unit availability and instruction dependencies, perform a merging and remapping of the at least two separate instruction groups to the at least a portion of functional units in a second stage.

14. (Original) The method of claim 13, further comprising: delivering the instructions to the portion of functional units following merging and remapping.

15. (Previously Presented) The method of claim 13, wherein the at least a portion of functional units execute instructions from the at least two instruction groups.

16. (Canceled)

17. (Original) The method of claim 13, wherein the instruction groups follow a simultaneous multi-threading structure.

18. (Original) The medium of claim 13, wherein the instruction groups are prioritized to prevent pipeline failures during execution of instructions.